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Term	Documents
(19 AND 7).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1
(L19 AND L7).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1

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<u>L23</u>	119 and 17	1	<u>L23</u>
<u>L22</u>	119 and 16	4	<u>L22</u>
<u>L21</u>	119 and 15	12	<u>L21</u>
<u>L20</u>	L19 and (instruction\$1 near4 cach\$3 or fill near3 buffer\$1)	12	<u>L20</u>
<u>L19</u>	L10 near35 (mux or multiplex\$5 or select\$5 or sel )	73	<u>L19</u>
<u>L18</u>	111 and 17	1	<u>L18</u>
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<u>L14</u>	14 and 16	5	<u>L14</u>
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<u>L11</u>	L10 and (mux or multiplex\$5 or select\$5 or sel ) near12 configura\$6	34	<u>L11</u>
<u>L10</u>	L8 near35 (size or width or length)	485	<u>L10</u>
<u>L9</u>	L8 near35 (mux or multiplex\$5 or select\$5 or sel ) near12 configura\$6	18	<u>L9</u>
<u>L8</u>	(plur\$7 or two or second) near5 (map\$6 or associat\$5) near8 (microinstruction\$1 or instruction\$1 or cod\$3)	16612	<u>L8</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L7</u>	(711/118-146)![CCLS]	7233	<u>L7</u>
<u>L6</u>	(712/212,213)[CCLS]	419	<u>L6</u>
<u>L5</u>	(712/2-300)[CCLS]	11598	<u>L5</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L4</u>	L3 and instruction\$1 near4 cach\$3	109	<u>L4</u>
<u>L3</u>	l2 and fill\$3 near4 buffer\$1	595	<u>L3</u>
<u>L2</u>	L1 and (mux or multiplex\$5 or select\$5 or sel ) near12 configura\$6	8900	<u>L2</u>
<u>L1</u>	(map\$6 or associat\$5) near8 (microinstruction\$1 or instruction\$1 or cod\$3)	138460	<u>L1</u>

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» Key

- IEEE JNL IEEE Journal or Magazine
- IEEE JNL IEE Journal or Magazine
- IEEE CNF IEEE Conference Proceeding
- IEEE CNF IEE Conference Proceeding
- IEEE STD IEEE Standard



**1. The direct-mapped instruction cache for ColdFire microprocessors**  
Tirumala, A.S.; Bibikar, V.J.;  
Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceedings., 1996 IEEE I  
Conference on  
7-9 Oct. 1996 Page(s):288 - 292  
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